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S22	88	717/155,156,159-161.ccls. and dependenc\$1 with (chang\$3 or modif\$4 or reconfigur\$3 or remov\$3 or delet\$3 or break\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/27 10:19
S23	62	(load or memory) near (operation or instruction) with (mov\$3 or reorder\$3) and dependenc\$1 with (chang\$3 or modif\$4 or reconfigur\$3 or remov\$3 or delet\$3 or break\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/27 10:20



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- 3 [Hardware/software resolution of pipeline hazards in pipeline synthesis of instruction set processors](#)

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- 4 [Memory Model = Instruction Reordering + Store Atomicity](#)



Arvind Arvind, Jan-Willem Maessen

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5 [Data speculation support for a chip multiprocessor](#)



Lance Hammond, Mark Willey, Kunle Olukotun

October 1998 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the eighth international conference on Architectural support for programming languages and operating systems ASPLOS-VIII**, Volume 32 , 33 Issue 5 , 11

Publisher: ACM Press